CLAIMS

What is claimed is:

1. A monolithic wireless device, the wireless device comprising:

a mixed-mode integrated circuit having a digital portion and an analog portion on a common die, wherein the analog portion comprises a radio frequency (RF) receiver circuit and wherein the digital portion comprises a signal processor in communication with the RF receiver circuit; and

a memory device in electronic communication with the mixed-mode integrated circuit, wherein the memory device is configured to store electronic instructions and data for the signal processor.

2. The wireless device of claim 1, wherein the memory device is stacked with the mixed mode integrated circuit on a substrate.

3. The wireless device of claim 2 wherein the memory device is direct bonded to the mixed mode integrated circuit.

4. The wireless device of claim 2 wherein the memory device is electrically coupled to the mixed mode integrated circuit by package pins disposed on the substrate.

5. The wireless device of claim 1 wherein the RF receiver circuit operates within a frequency band and wherein the digital portion comprises a clock signal having a clock frequency that is provided to the signal processor.

6. The wireless device of claim 5 wherein the clock frequency is configured such that neither the clock frequency nor any harmonics of the clock frequency lie within the frequency band.

7. The wireless device of claim 6 wherein the RF receiver circuit comprises a filter tuned to remove a harmonic of the clock frequency from an analog signal propagating in the analog portion.

8. The wireless device of claim 5 wherein the RF receiver circuit comprises:
an amplifier configured to receive an analog signal from an antenna;
a mixer configured to mix the analog signal with an oscillator signal having a frequency within the frequency band; and
an analog-to-digital converter configured to provide a digital equivalent of the analog signal to the signal processor.

9. The wireless device of claim 8 wherein the amplifier is a differential amplifier comprising at least two differential inputs.

10. The wireless device of claim 9 wherein the RF receiver circuit further comprises a filter coupled to one of the at least two differential inputs and tuned to remove at least a portion of the clock frequency from an analog signal propagating in the analog portion.

11. The wireless device of claim 1 wherein the analog portion and the digital portion are at least partially separated by a conducting trench in the common die.

12. The wireless device of claim 11 wherein the conducting trench is connected to an electrical ground.

13. The wireless device of claim 1 wherein the digital portion comprises a plurality of conducting members proximate to a surface of the common die to thereby form a Faraday cage about the digital portion.

14. A monolithic receiver for a global positioning system (GPS), the receiver comprising:
a substrate;
a mixed-mode integrated circuit coupled to the substrate and having a digital portion and an analog portion on a common die, wherein the analog portion comprises an RF receiver circuit operating within a frequency band and wherein the digital portion comprises a signal processor in communication with the RF receiver circuit, wherein the digital

portion comprises a clock signal having a clock frequency provided to the signal processor, and wherein the clock frequency is selected such that neither the clock frequency nor any harmonics of the clock frequency lie within the frequency band; and

a memory device stacked with the mixed-mode integrated circuit opposite the substrate and configured in electronic communication with the mixed-mode integrated circuit, wherein the memory device is configured to store electronic instructions and data for the signal processor.

15. The receiver of claim 14 wherein the analog portion and the digital portion are at least partially separated by a conducting trench in the common die, and wherein the conducting trench is connected to an electrical ground.

16. A wireless receiver provided on a common die in communication with an antenna, the wireless receiver comprising:

a system bus disposed on the common die;

an analog portion coupled to the system bus and comprising a radio frequency (RF) receiver circuit configured to receive an analog signal from the antenna and to provide a digital representation of the analog signal therefrom;

an acquisition module configured to communicate with the RF receiver circuit via the system bus and to thereby receive the digital representation of the analog signal, wherein the acquisition module is further configured to process the digital representation to thereby extract data from the analog signal;

a processor coupled to the system bus, wherein the processor is configured to control the RF receiver and the acquisition module, and to process the data from the acquisition module to thereby provide an output of the wireless receiver.

17. The wireless receiver of claim 16 further comprising an interface module coupling the processor to the system bus.

18. The wireless receiver of claim 17 wherein the interface module comprises a bus controller, a clock generator and an external interface for the wireless receiver.

19. The wireless receiver of claim 18 wherein the clock generator is operable to produce a system clock signal to the processor and the acquisition module.

20. The wireless receiver of claim 16 further comprising an interrupt controller disposed on the common die and coupled to the data bus, wherein the interrupt controller is operable to provide interrupt requests received via the system bus to the processor.

21. The wireless receiver of claim 16 further comprising an interface from the system bus to an external memory stacked with the common die.

22. The wireless receiver of claim 16 further comprising a boot module comprising a sequence of logic gates in communication with the system bus and operable to provide a boot sequence implemented in the sequence of logic gates to the processor.

23. The wireless receiver of claim 16 further comprising an automatic level control (ALC) module coupling the analog portion to the system bus, wherein the ALC module is configured to providing blanking and level control to the RF receiver in response to signals received from the processor via the system bus.

24 The wireless receiver of claim 16 further comprising clock generating circuitry configured to produce a system clock signal for the processor and the acquisition module as a function of an external reference.

25. The wireless receiver of claim 16 further comprising clock generating circuitry configured to produce a system clock signal for the processor and the acquisition module as a function of a selected one of a plurality of external references.

26. The GPS receiver of claim 16 further comprising a memory in a stacked configuration with the common die.

27. The wireless receiver of claim 26 further comprising a second memory in the stacked configuration with the common die.

28. The wireless receiver of claim 16 further comprising a filter in a stacked configuration with the common die.

29. A monolithic die for a wireless receiver stacked with a memory and electrically coupled to an antenna, the monolithic die comprising:

a system bus disposed on the die;

an analog portion coupled to the system bus and comprising a radio frequency (RF) receiver circuit configured to receive an analog signal from the antenna and to provide a digital representation of the analog signal therefrom;

an acquisition module configured to communicate with the RF receiver circuit via the system bus and to thereby receive the digital representation of the analog signal, wherein the acquisition module is further configured to process the digital representation to thereby extract data from the analog signal;

a processor coupled to the system bus, wherein the processor is configured to control the RF receiver and the acquisition module, and to process the data from the acquisition module to thereby provide an output of the wireless receiver.

30. A monolithic wireless device contained within a package, the device comprising:

a substrate disposed within the package;

a mixed-mode integrated circuit coupled to the substrate and having a digital portion and an analog portion on a common die; and

a memory stacked with the mixed-mode integrated circuit within the package, wherein the memory is in electronic communication with the mixed-mode integrated circuit to implement the wireless device.

31. The wireless device of claim 30 wherein the memory is direct bonded to the mixed mode integrated circuit.

32. The wireless device of claim 30 wherein the memory is electrically coupled to the mixed mode integrated circuit by package pins disposed on the substrate.

33. A monolithic wireless device contained within a package, the device comprising:

means for receiving wireless signals;

means for processing the wireless signals received at the receiving means, the processing means comprising a digital portion and an analog portion on a common die; and

means for storing data and instructions for the processing means, wherein the storing means is stacked with the processing means within the package.